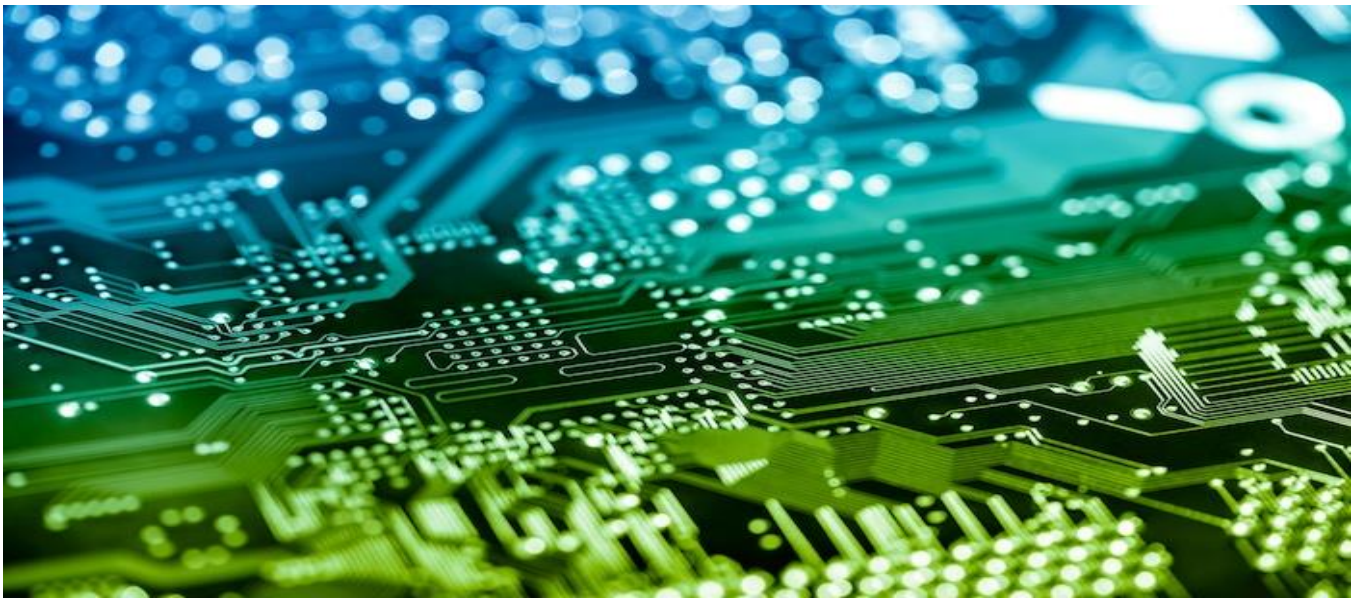
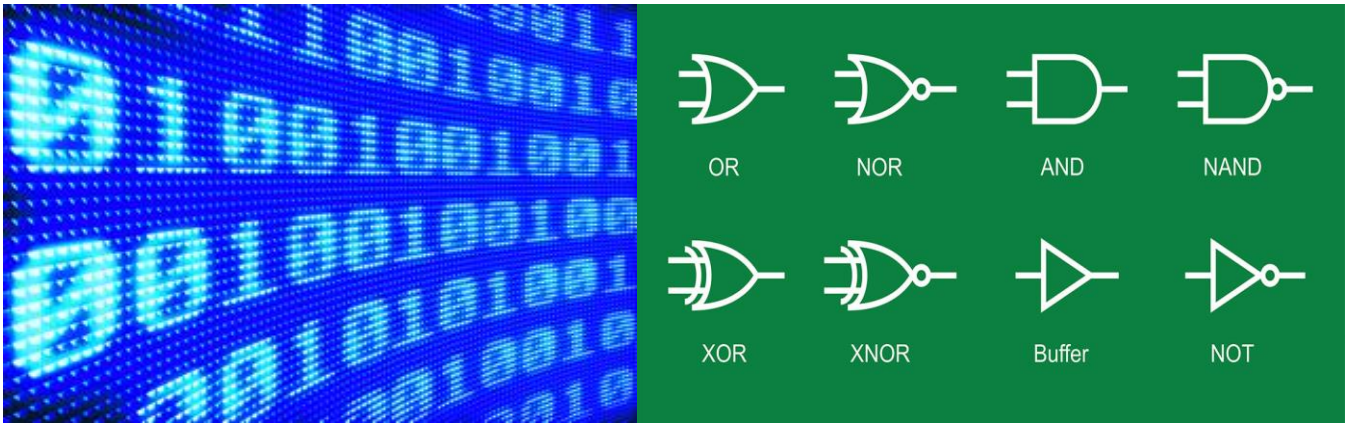
PRINCIPLES OF DIGITAL ELECTRONICS LAB

Department of Electrical and Electronics Engineering





GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

(Autonomous)

(Approved by A.I.C.T.E and Affiliated to JNTU) Bachupally, Kukatpally, HYDERABAD 500090.

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY
(Autonomous)

Principles of Digital Electronics Lab Record

Name: ……

Reg no:……..

Course: B.Tech. II Yr II Semester

Branch: EEE

CERTIFICATE

This is to certify that it is a bonafide record of practical work done in the Principles Digital Electronics Lab in the II semester of II year during _____by Mr. /Ms._____

Reg. No._____

Internal Examiner
Signature

External Examiner
Signature

CONTENTS

1. INTRODUCTION TO ANALOG DISCOVERY KIT

Overview

The Digilent Analog Discovery , developed in conjunction with Analog Devices Inc., is a multi- function instrument that can measure, record and generate analog and digital signals.

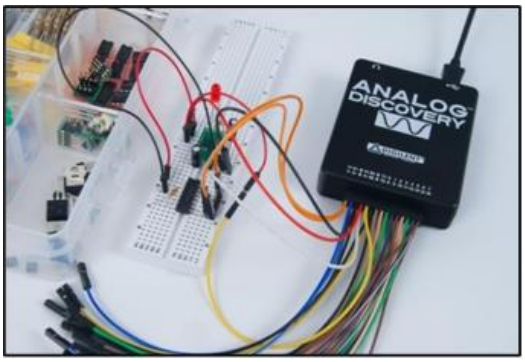


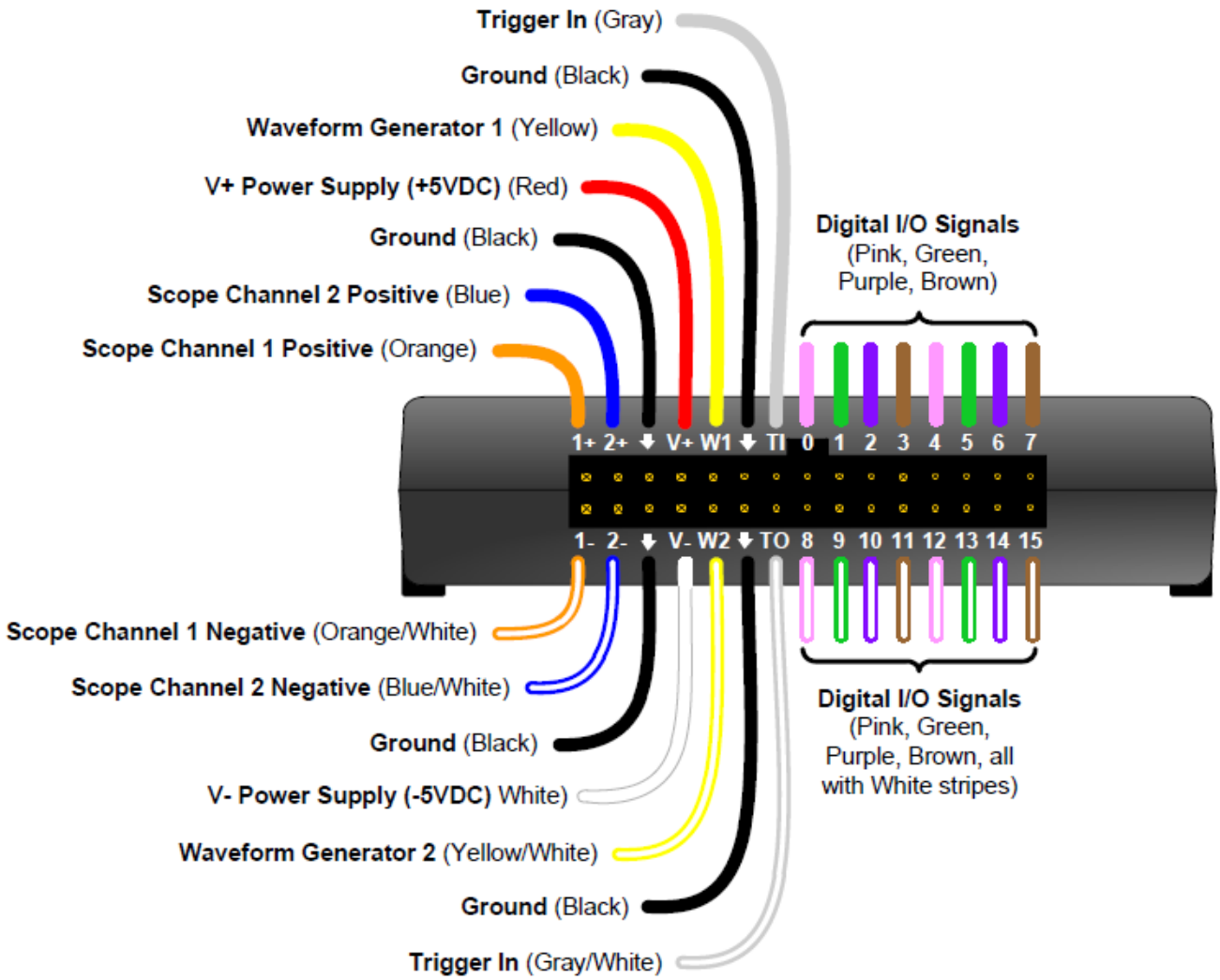
Figure: Analog Discovery used in a circuit design experiment

The small, portable and low-cost Analog Discovery (above Figure) was created so that engineering students could work with analog and digital circuits anytime, anywhere - right from their PC. The Analog Discovery's analog and digital inputs and outputs connect to a circuit using simple wire probes. Inputs and outputs are controlled using the free PC- based Waveforms software that can configure the Discovery to work as any one of several traditional instruments. Instruments include:

- Two channel oscilloscope (1MΩ, ±25V, differential, 14 bit, 100Msample/sec, 5MHz bandwidth);
- Two channel arbitrary function generator (22Ω, ±5V, 14 bit, 100Msample/sec, 5MHz bandwidth);
- Stereo audio amplifier to drive external headphones or speakers with replicated AWG signals;
- 16-channel digital logic analyzer (3.3V CMOS, 100Msample/sec)*;
- 16-channel pattern generator (3.3V CMOS, 100Msample/sec)*;
- 16-channel virtual digital I/O including buttons, switches and LEDs –good for logic trainer applications*;
- Two input/output digital trigger signals for linking multiple instruments (3.3V CMOS);
- Two power supplies (+5V at 50mA, -5V at 50mA).
- Single channel voltmeter (AC, DC, ±25V);
- Network analyzer – Bode, Nyquist, Nichols transfer diagrams of a circuit. Range: 1Hz to 10MHz;
- Spectrum Analyzer - power spectrum and spectral measurements (noise floor, SFDR, SNR, THD, etc.);
- Digital Bus Analyzers (SPI, I2C, UART, Parallel);

The Analog Discovery was designed for students in typical university-based circuits and electronics classes. Its features and specifications, including operating from USB power, a small and portable form factor, and the ability to be used by students in a variety of environments at low cost, are based directly on inputs from many professors at many universities. Meeting all the requirements proved challenging, and resulted in some new and innovative circuits. This document is a reference for the Analog Discovery's electrical functions and operations. This reference also provides a description of the hardware's features and limitations. It is not intended to provide enough information to enable complete duplication of the Analog Discovery, or to allow users to design custom configurations for programmable parts in the design.

The pin-out terminals of Analog Discovery Kit (AD Kit) is shown below



2.STEPS TO RUN WAVEFORM SOFTWARE

Step1: Open the "Waveform" software from the start menu of the windows desktop

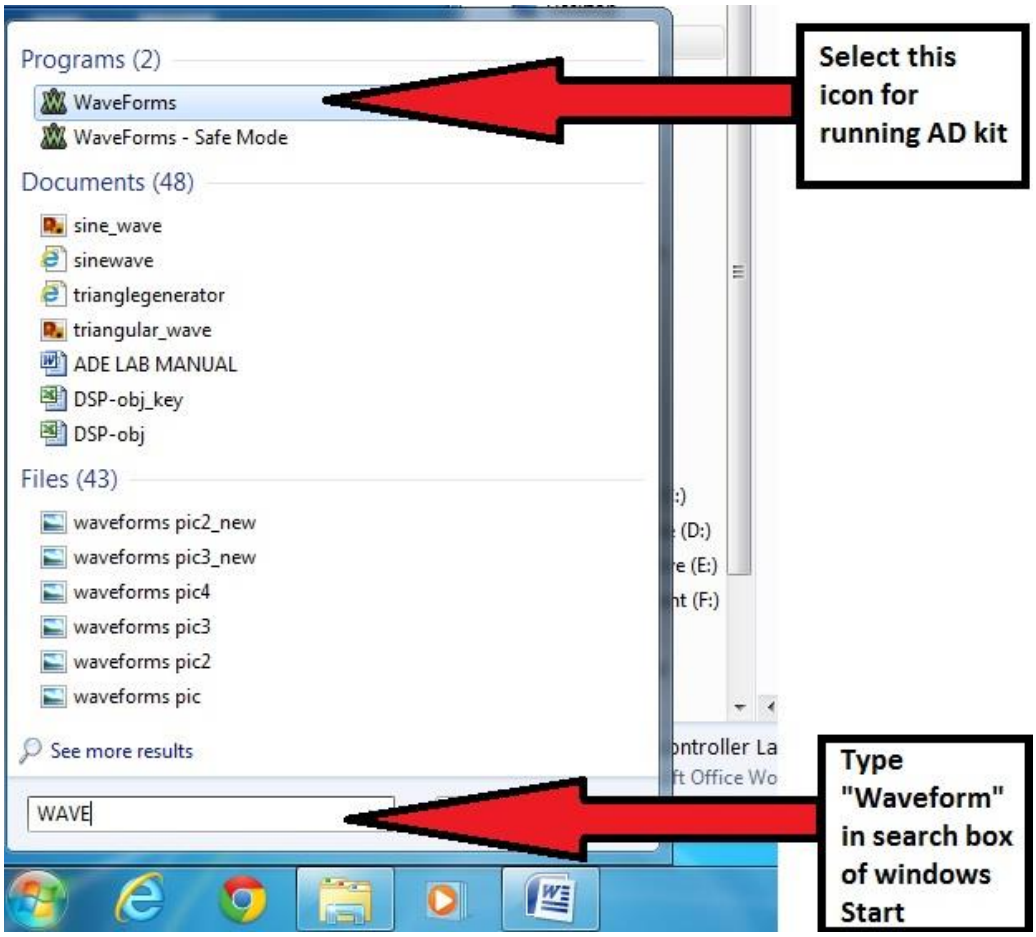


Figure: Showing the selection of Waveform software from the start menu

Step2: Each block representation of Waveform software

"in" -To check waveforms at the output terminals of the hardware connections done on Bread board "in" is selected

"out"- To give different input signals to the circuit done on the Bread board "out" is selected

"voltage"-This option is selected to apply +Vcc and –Vcc to the circuit connections done on Bread board

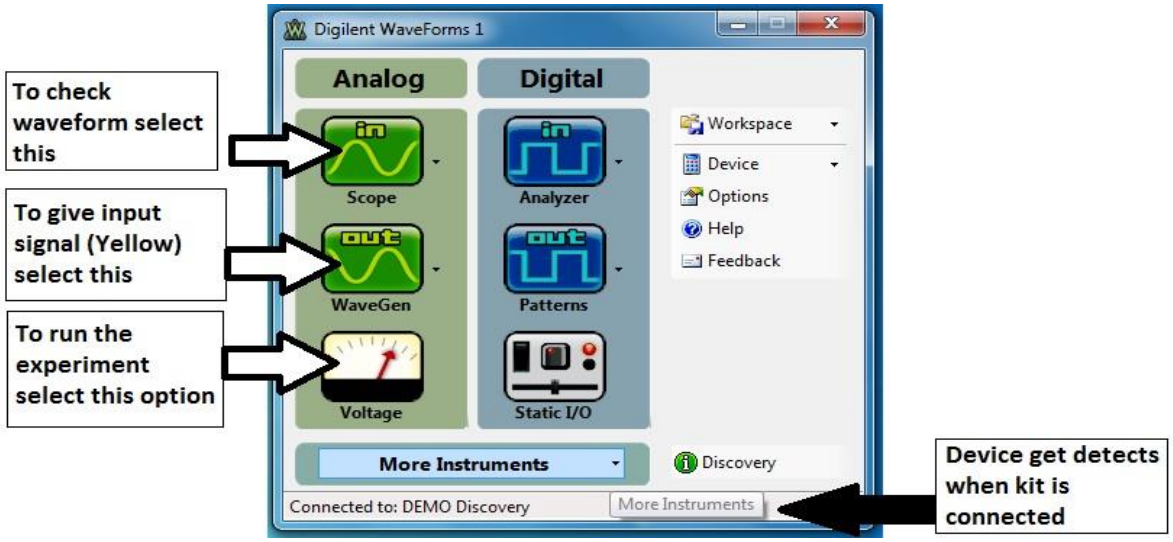


Figure: showing the Window of Waveform software

Step 3: The window shown below is obtained when "in" is selected from the "Waveform" software. Two waveforms can be seen at one time (one is "orange" and the other is "Blue"). The right side window shows the settings of different waveforms who's Y and X axis can be set. After selecting the required options, click the "Run" button on Top left side of the Window to see the obtained output of the circuit connected on the Bread board.

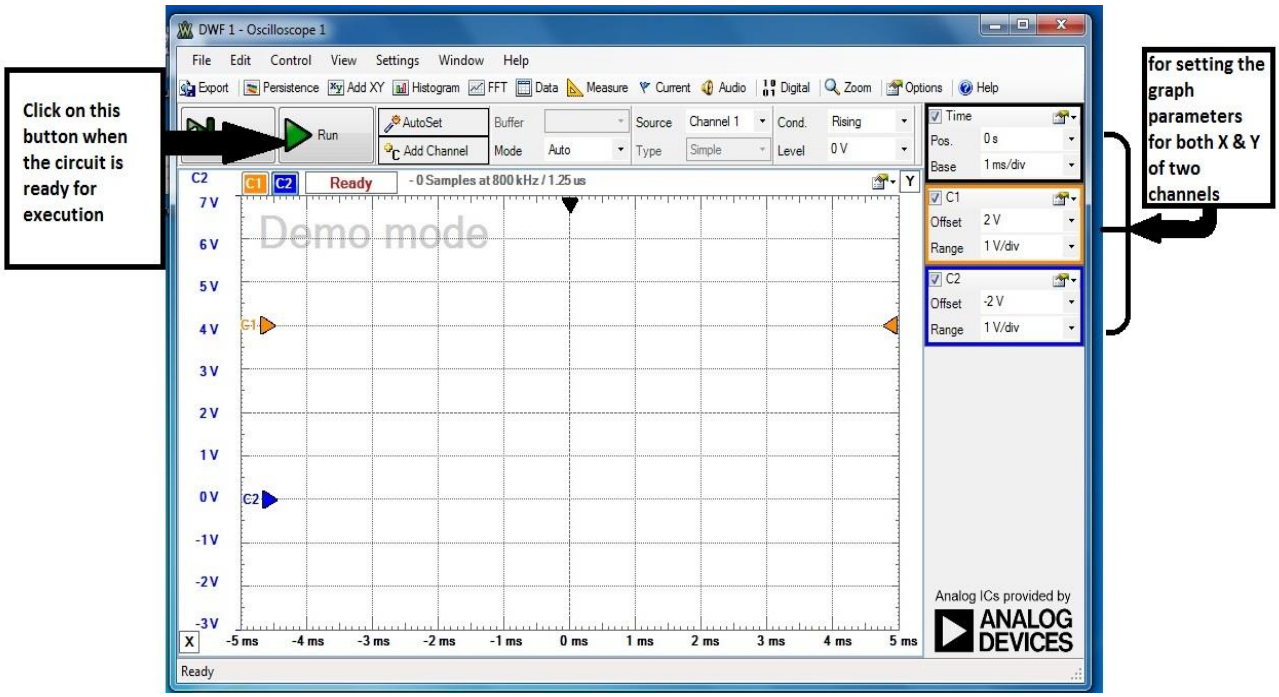


Figure: Shows the "in" window of "Waveform" software

Step4: "Out" tab of Waveform software is used for selecting the types of waveforms like-sinusoidal, square, triangular, trapezoidal, random signal of different frequencies from this window. The signal selected from this window is given as input signal to the circuit connected on the Bread board. After making the required settings click on the "Run AWG1" option from the window.

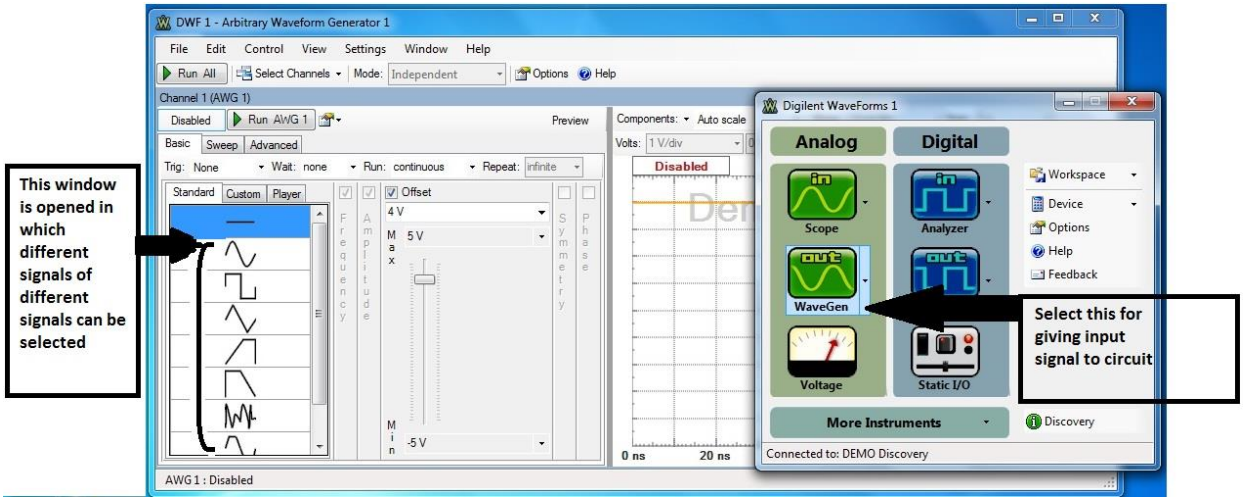


Figure: The "Out" window of Waveform in which different waveforms can be given as input

Step5: "Voltage" is selected for giving the input voltage of either +Vcc (Constant +5V) or –Vcc (Constant -5V) or both. When the "Power is ON/OFF" is selected the respective voltages are applied to the circuit connected.

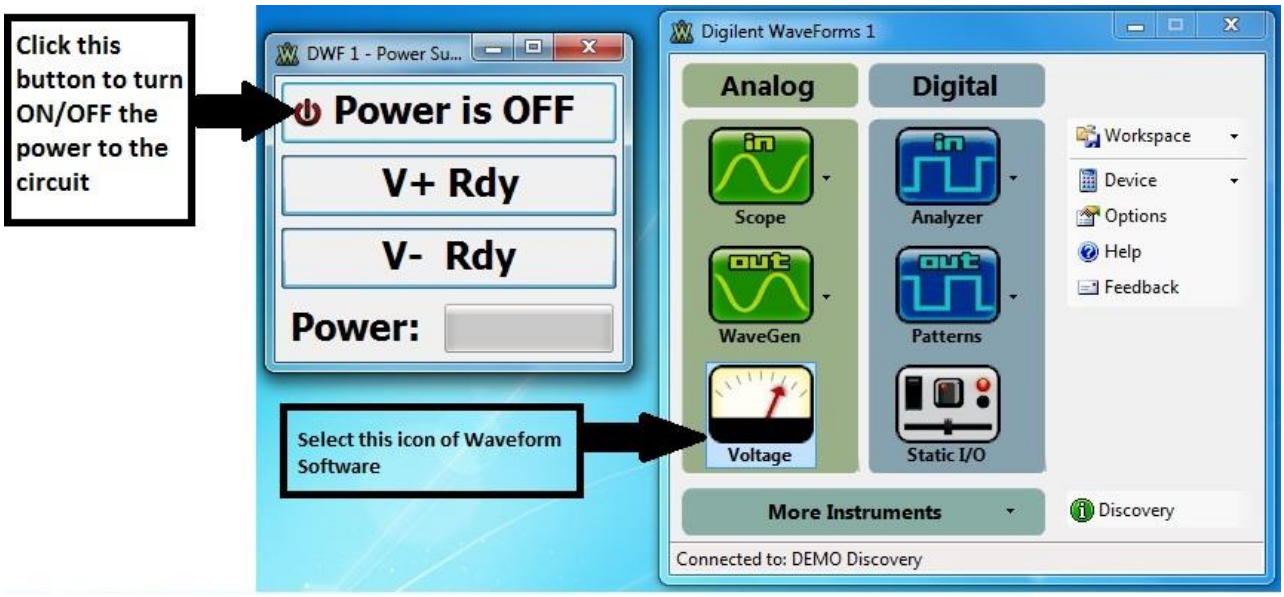


Figure: The "Voltage" window of Waveform helps to run the ADE kit

3. Logic Gates

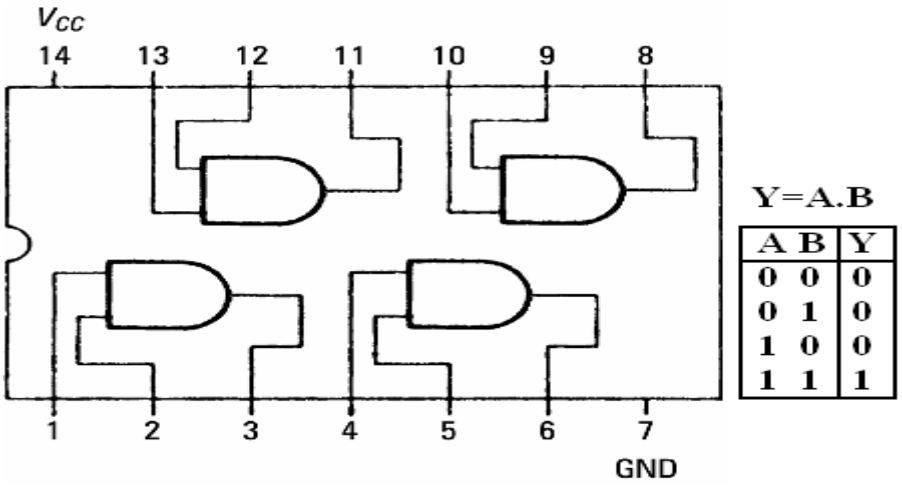
Aim: To study the basic Logic Gates and verify their Truth Tables - AND, OR, NOT, NAND, NOR, Exclusive OR: XOR, Exclusive NOR: XNOR Gates.

Apparatus: Analog Discovery Kit
Bread board
Logic gates / IC's (No. specified or its equivalent GATES)

Theory: Logic gates are electronic circuits which perform logical functions/digital information sharing on one or more inputs carrying information/bits to produce one output. There are seven basic logic gates. **Truth Table** is the input combinations of a logic gate that are written in a table and their corresponding outputs represented along them. Logic gates and their working are described.

AND Gate

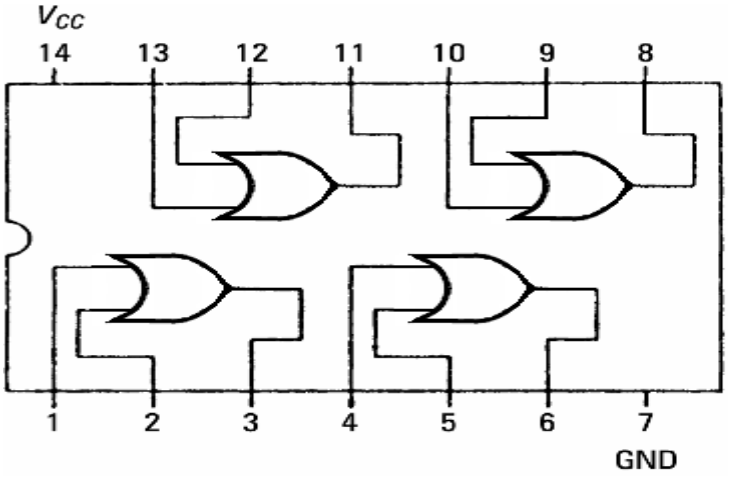
AND gate (7408) consists of minimum TWO inputs (depends upon the IC model), produces an output of 1, if and only if all its inputs are 1; or else the output is 0.



IC 7408

OR Gate

OR gate (7432) consists of minimum TWO inputs (depends upon the IC model) produces an output 1, when any one or all its inputs are 1; otherwise the output is 0.



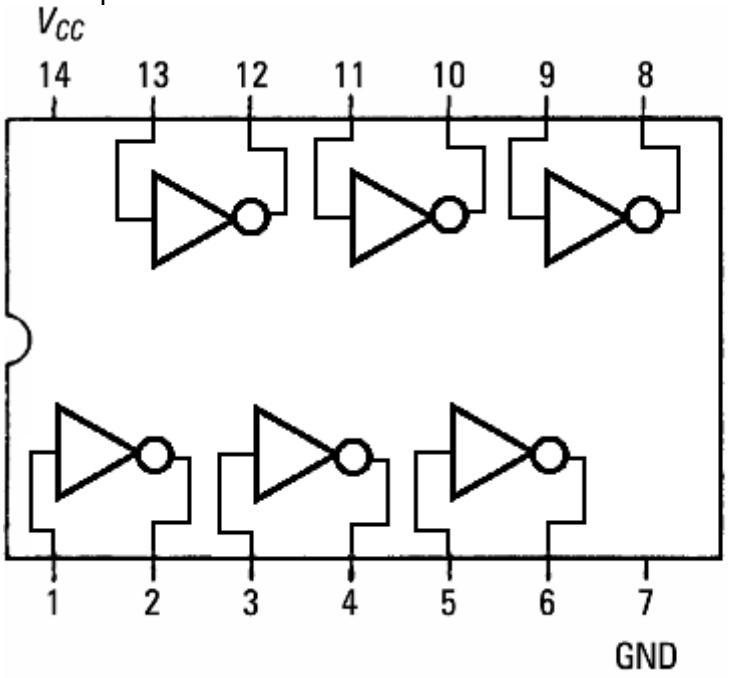
Y=A+B

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

IC 7432

NOT Gate

NOT gate (7404) produces the complement of its input. This gate is also called an INVERTER. It always has one input and one output. Its output is 0 when input is 1 and output is 1 when input is 0.



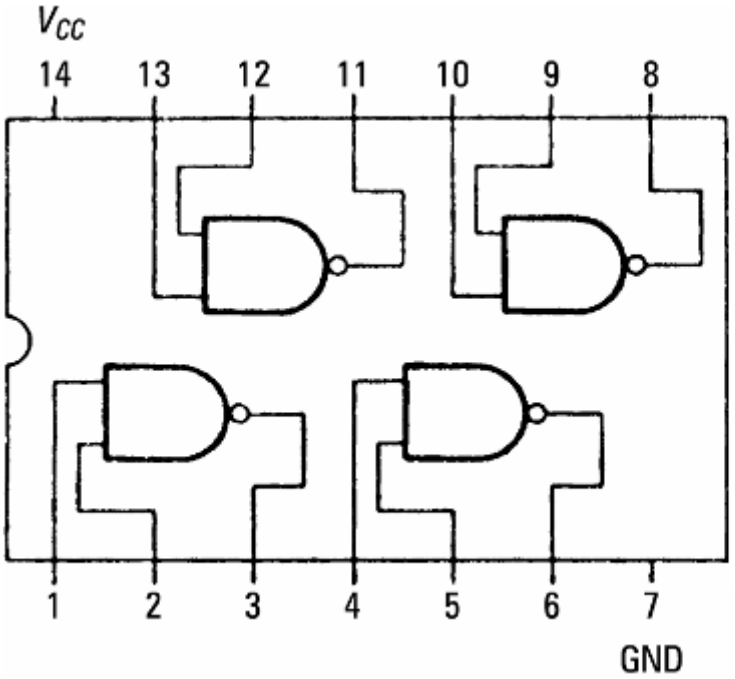
$Y=\overline{A}$

A	Y
0	1
1	0

IC 7404

NAND Gate

NAND Gate (7400) is a combination of AND, NOT gates in series, this combination will work as NOT-AND or NAND gate. Its output is 1 when any or all inputs are 0, otherwise output is 1.



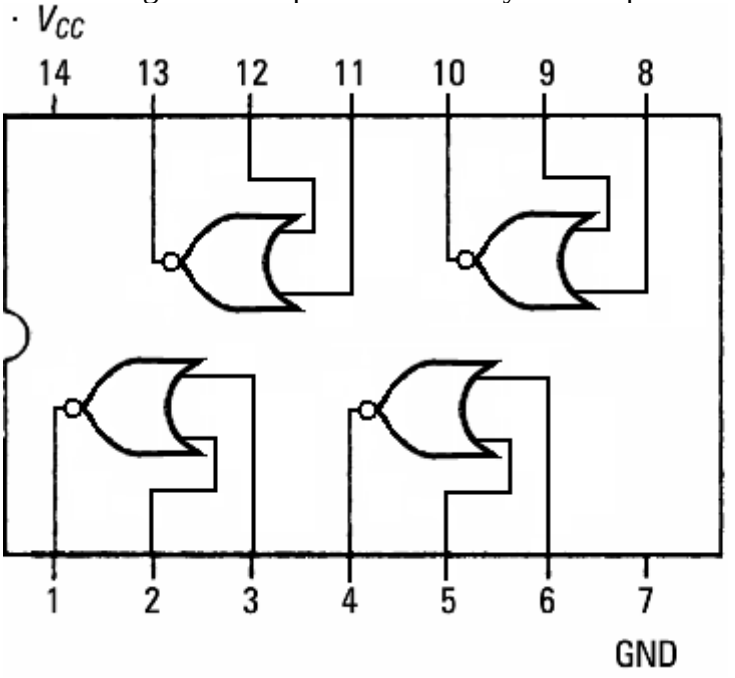
$Y=\overline{A.B}$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

IC 7400

NOR Gate

NOR gate (7402) is a combination of OR, NOT gates in series, this combination will work as NOT-AND or NAND gate. Its output is 0 when any or all inputs are 1, otherwise output is 0.



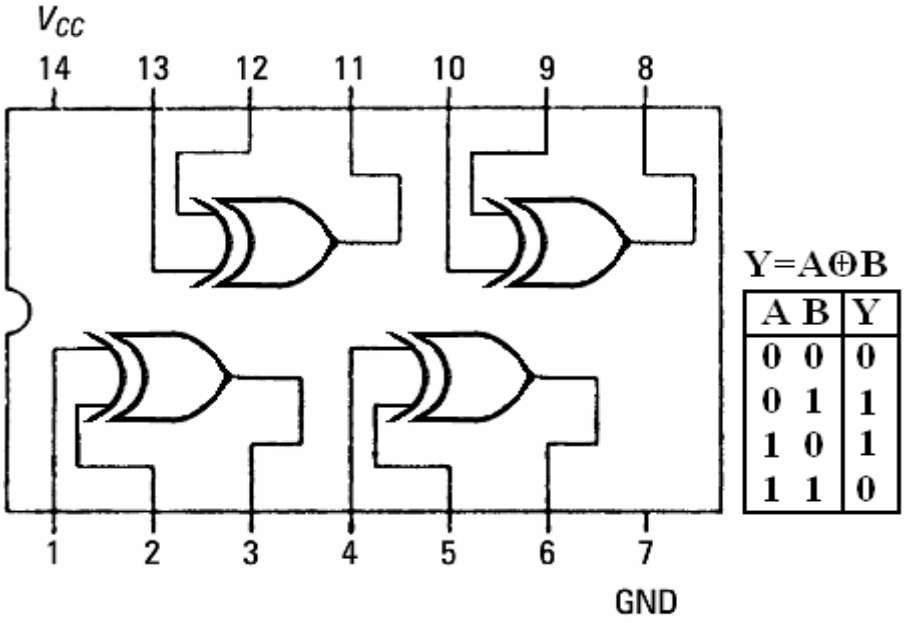
$Y=\overline{A+B}$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

IC 7402

Exclusive OR (X-OR) Gate

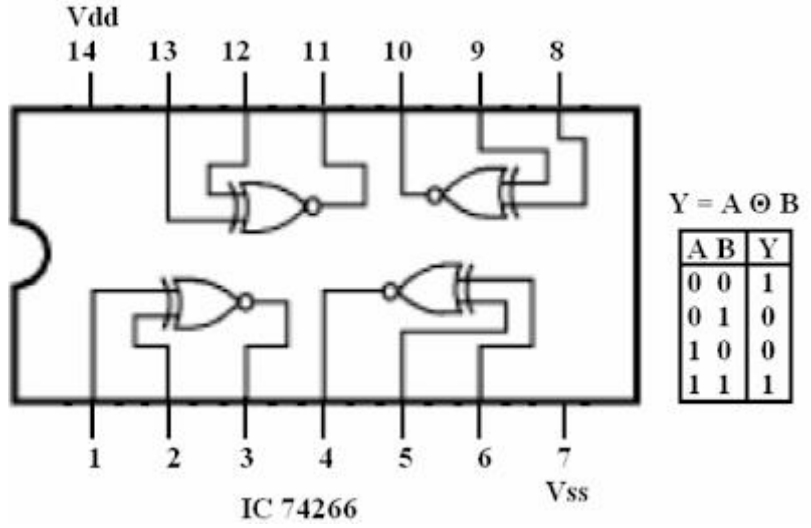
X-OR (7486) gate produces an output as 1, when number of 1's at its inputs is **odd**, otherwise output is 0. It has two inputs and one output.



IC 7486

Exclusive NOR (X-NOR) Gate

X-NOR (74266) gate produces an output as 1, when number of 1's at its inputs is **not odd**, otherwise output is 0. It has two inputs and one output.



Procedure:

1. Interface the Analog Discovery Kit.
2. Terminals used from Analog Discovery kit are: any digital connections from 1 to 16 available from the Kit to Input terminals of Logic Gate and Vss (Red from AD Kit) and Vdd (Ground from AD Kit)
3. Complete the connections as per the terminals mentioned in Analog Discovery Kit with IC.
4. Connect the inputs of each logic gate with Analog Discovery Kit and obtain the Timing diagrams.

5. Apply various input combinations, observe and record the output for each pattern/combination.
6. Verify the Truth Table for each input/ output combination with the recorded values
7. Repeat the procedure for all other Logic Gates.

Result:

The Logic Gates are studied and their respective truth tables are verified.

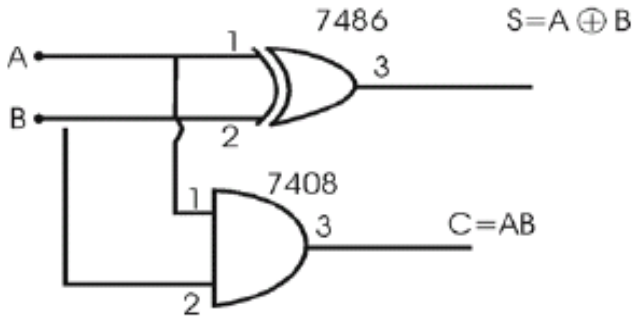
4. Half Adder and Full Adder

Aim: To design and implement Half Adder and Full Adder circuits using basic logic gates and verify their truth tables.

Apparatus: Analog Discovery Kit
Bread board
Logic gates / IC's (No. specified or its equivalent GATES):
IC 7486, IC 7432, IC 7408, etc
Connecting Wires

Circuit Diagram:-

Half Adder using basic gates:-

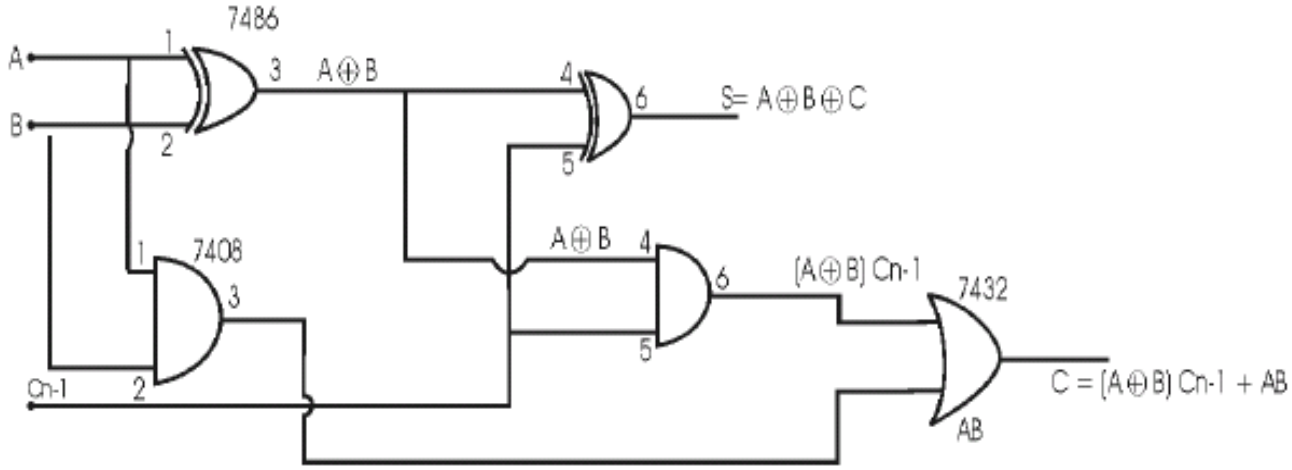


$S = \overline{A}B + A\overline{B}$

$S = A \oplus B$

$C = AB$

Full Adder using basic gates:-



Procedure:

1. Interface the Analog Discovery Kit.
2. Terminals used from Analog Discovery kit are: any digital connections from 1 to 16 available from the Kit to Input terminals of Logic Gates and Vss (Red from AD Kit) and Vdd (Ground from AD Kit)
3. Complete the connections as per the terminals mentioned in Analog Discovery Kit with IC.
4. Connect the inputs of each logic gate with Analog Discovery Kit and obtain the Timing diagrams.

5. Apply various input combinations, observe and record the output for each pattern/combination.
6. Complete the Truth Table for each input/output combination and justify with the operation.

Truth Table

Half Adder					
A	B	S	C	S(V)	C(V)
	0	0	0		
0	1	1	0		
1	0	1	0		
1	1	0	1		

Full Adder						
A	B	Cn-1	S	C	S(V)	C(V)
0	0	0	0	0		
0	0	1	1	0		
0	1	0	1	0		
0	1	1	0	1		
1	0	0	1	0		
1	0	1	0	1		
1	1	0	0	1		
1	1	1	1	1		

Result:

Thus the Half Adder and Full Adder circuits are designed and the truth tables are verified.

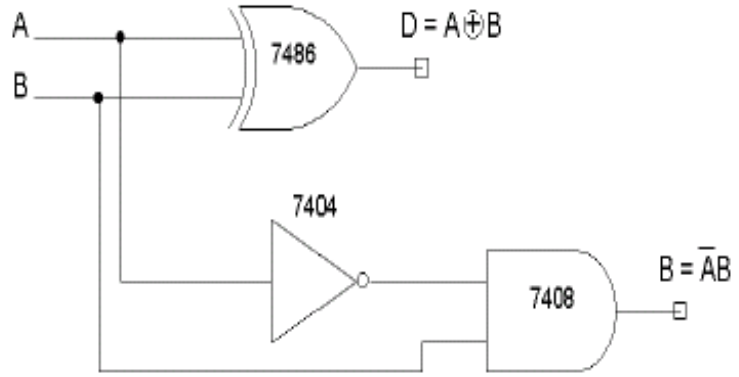
5. Half Subtractor and Full Subtractor

Aim: To design and implement Half Subtractor and Full Subtractor circuits using basic logic gates.

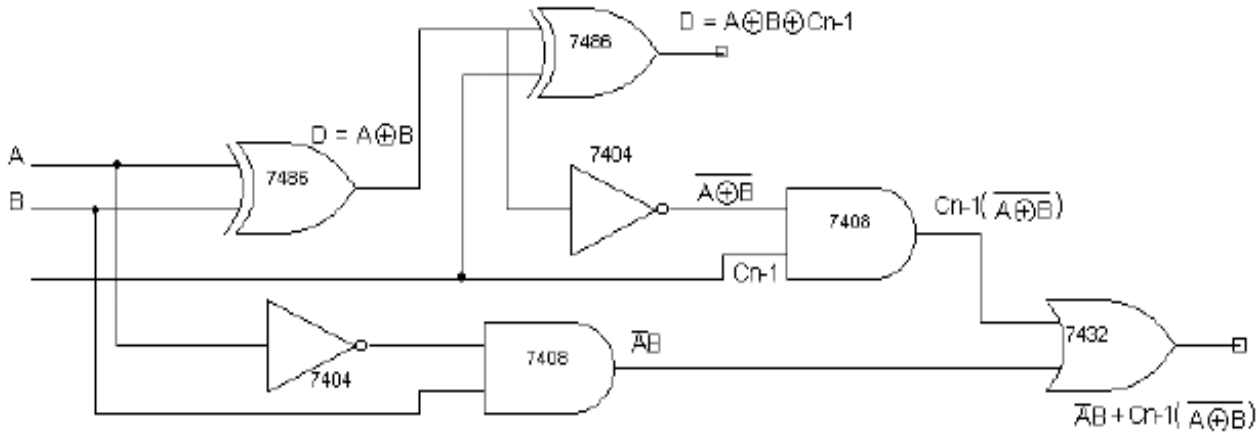
Apparatus: Analog Discovery Kit
Bread board
Logic gates / IC's (No. specified or its equivalent GATES):
IC 7486, IC 7432, IC 7408, IC 7404, etc
Connecting Wires

Circuit Diagrams:

Using X – OR and Basic Gates (a)Half Subtractor



Full Subtractor



Procedure:

1. Interface the Analog Discovery Kit.
2. Terminals used from Analog Discovery kit are: any digital connections from 1 to 16 available from the Kit to Input terminals of Logic Gates and Vss (Red from AD Kit) and Vdd (Ground from AD Kit)
3. Complete the connections as per the terminals mentioned in Analog Discovery Kit with IC.

4. Connect the inputs of each logic gate with Analog Discovery Kit and obtain the Timing diagrams.
5. Apply various input combinations, observe and record the output for each pattern/combination.
6. Complete the Truth Table for each input/output combination and justify with the operation.

Truth Table

Half Subtractor					
A	B	D	B	D(V)	B(V)
0	0	0	0		
0	1	1	1		
1	0	1	0		
1	1	0	0		

Full Subtractor						
A	B	Cn-1	D	B	D(v)	B(v)
0	0	0	0	0		
0	0	1	1	1		
0	1	0	1	1		
0	1	1	0	1		
1	0	0	1	0		
1	0	1	0	0		
1	1	0	0	0		
1	1	1	1	1		

Result:

Thus the Half Subtractor and Full Subtractor circuits are designed and the truth tables are verified.

6. Design and implementation of parallel adder/subtractor

Aim: To design and implement a 4-bit parallel adder/ subtractor circuit.

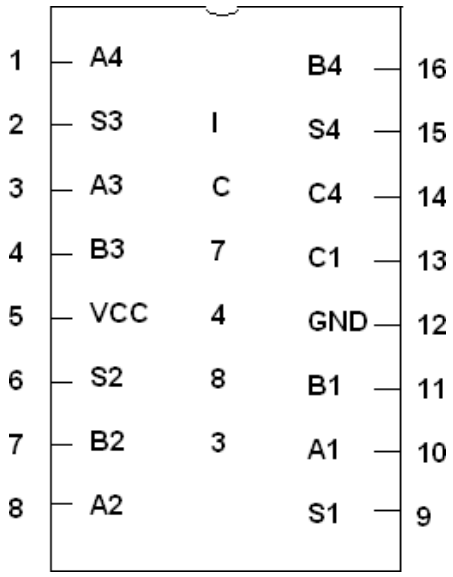
Apparatus: Analog Discovery Kit
Bread board
Logic gates / IC's (No. specified or its equivalent GATES):
4-bit adder (IC 7483), X-OR gates (IC 7486)
Connecting Wires

Theory:

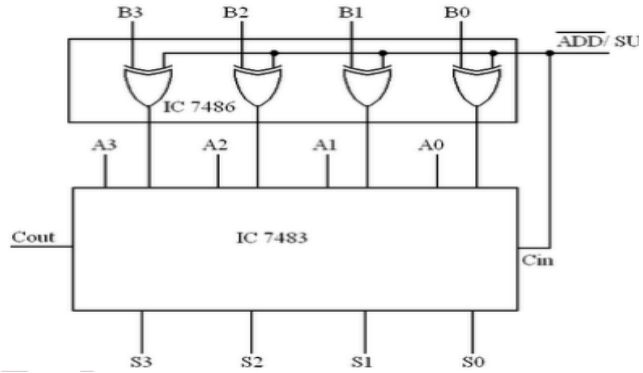
The addition and subtraction operation can be combined into one circuit with one common binary adder. The mode input M controls the operation. When M=0, the circuit is adder circuit. When M=1, it becomes subtractor.

IC 7483 is a 4 bit adder. In binary, subtraction can be performed by using 2's complement method. In this method negative number is converted into its 2's complement and it is added to the other number. The result of this addition is the subtraction of origin numbers. If we modify the adder circuit, such that 2's complement and simple representation are presented, we can perform addition subtraction as required. X-OR gate is used as a controlled inverter/ buffer for this purpose. Use it as buffer for addition and inverter for subtraction.

PIN Diagram IC 7483:



Circuit Diagram



Procedure:

1. Connect the IC 7483 and IC 7486 as per diagram.
2. Connect all A's and all B's to logic sources, S's to logic indicators.
3. Connect Cin to logic 0, this will set the circuit for addition.
4. Give various input combinations, verify adder operation. Here Cout is MSB of addition.
5. Connect Cin to logic 1, this will set the circuit for subtraction by 2's complement method.
6. Give various input combinations and observe outputs. Here Cout is neglected (2's complement subtraction)

Truth Table:

Input Data A				Input Data B				Addition					Subtraction				
A4	A3	A2	A1	B4	B3	B2	B1	C	S4	S3	S2	S1	B	D4	D3	D2	D1
1	0	0	0	0	0	1	0	0	1	0	1	0	1	0	1	1	0
1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0
0	0	1	0	1	0	0	0	0	1	0	1	0	0	1	0	1	0
0	0	0	1	0	1	1	1	0	1	0	0	0	0	1	0	1	0
1	0	1	0	1	0	1	1	1	0	0	1	0	0	1	1	1	1
1	1	1	0	1	1	1	1	1	1	0	1	0	0	1	1	1	1
1	0	1	0	1	1	0	1	1	0	1	1	1	0	1	1	0	1

Result:

Thus the 4-bit adder/subtractor circuit is implemented.

7. Multiplexer

Aim:

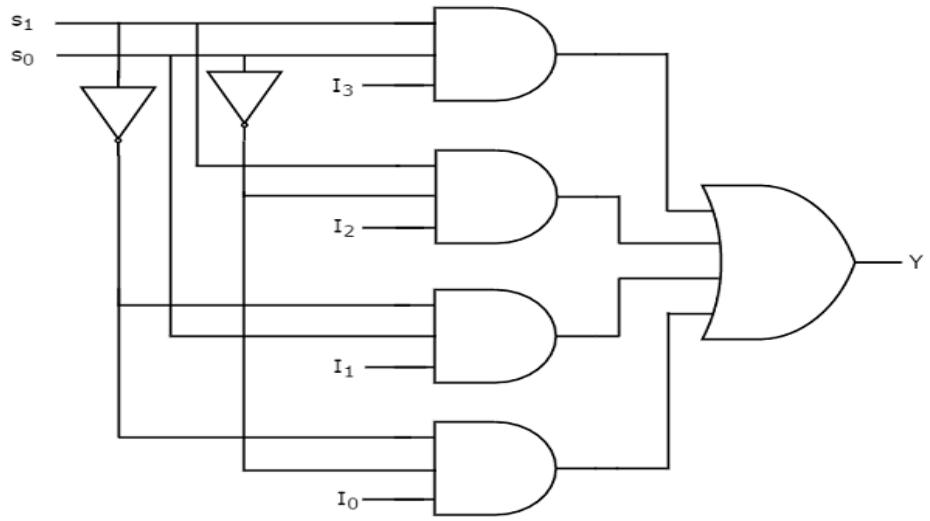
To design and implement 4X1 Multiplexer using Logic Gates.

Apparatus: Analog Discovery Kit
Bread board
Logic gates / IC's (No. specified or its equivalent GATES):
IC 7404, IC 7408, IC 7432
Connecting Wires

Theory:

A digital multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally there are 2^n input lines and n selection lines whose bit combination determine which input is selected. In the 4X1 Multiplexer since there are 4 input lines, 2 select lines are required.

Circuit Diagram:



Truth Table:

Select Lines		Output
S1	**S0**	**Y**
0	0	I0
0	1	I1
1	0	I2
1	1	I3

Procedure:

1. Interface the Analog Discovery Kit.
2. Complete the connections as per the terminals mentioned in Analog Discovery Kit with IC.
3. Connect the inputs of each logic gate with Analog Discovery Kit and obtain the Timing diagrams.
4. Apply various input combinations, observe and record the output for each pattern/combination.
5. Complete the Truth Table for each input/output combination and justify with the operation.

Result:

The 4X1 Multiplexer implemented and truth table verified.

8. Decoder

Aim:

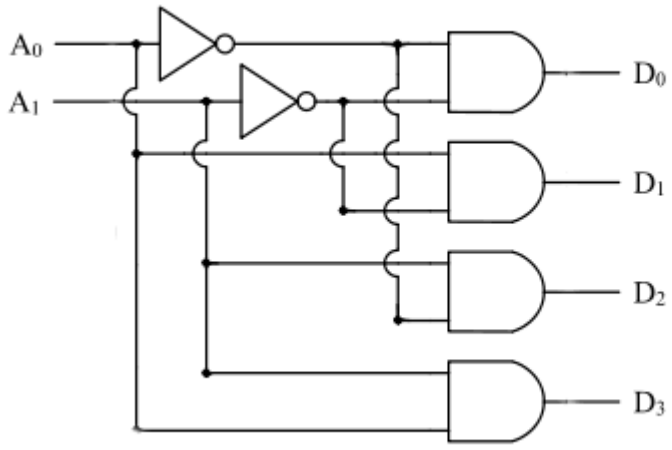
To design and implement 2X4 Decoder using Logic Gates.

Apparatus: Analog Discovery Kit
Bread board
Logic gates / IC's (No. specified or its equivalent GATES):
IC 7404, IC 7411
Connecting Wires

Theory:

Decoder is a combinational circuit that has 'n' input lines and maximum of 2^n output lines. One of these outputs will be active High based on the combination of inputs present, when the decoder is enabled. That means decoder detects a particular code. The outputs of the decoder are nothing but the min terms of 'n' input variables, when it is enabled.

Circuit Diagram:



Truth Table

A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Equations

$D_0 = \overline{A_1} \cdot \overline{A_0}$

$D_1 = \overline{A_1} \cdot A_0$

$D_2 = A_1 \cdot \overline{A_0}$

$D_3 = A_1 \cdot A_0$

Procedure:

1. Interface the Analog Discovery Kit.
2. Complete the connections as per the terminals mentioned in Analog Discovery Kit with IC.
3. Connect the inputs of each logic gate with Analog Discovery Kit and obtain the Timing diagrams.
4. Apply various input combinations, observe and record the output for each pattern/combination.
5. Complete the Truth Table for each input/output combination and justify with the operation.

Result:

The 2X4 Decoder implemented and truth table verified.

9. Magnitude Comparator

Aim:

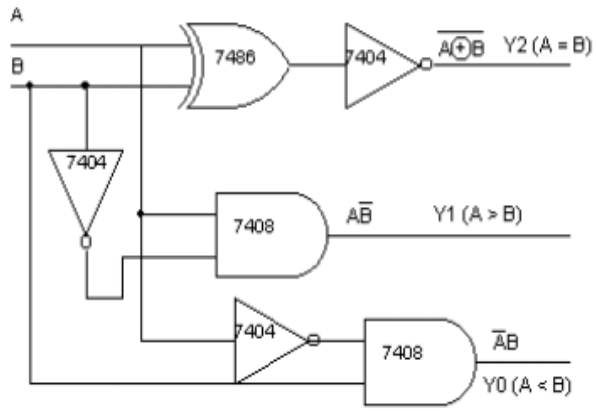
To design and implement One bit and Four bit Comparator Circuits.

Apparatus:

Analog Discovery Kit
Bread board
Logic gates / IC's (No. specified or its equivalent GATES):
IC 7486, IC 7404, IC 7408, IC 7485etc.
Connecting Wires

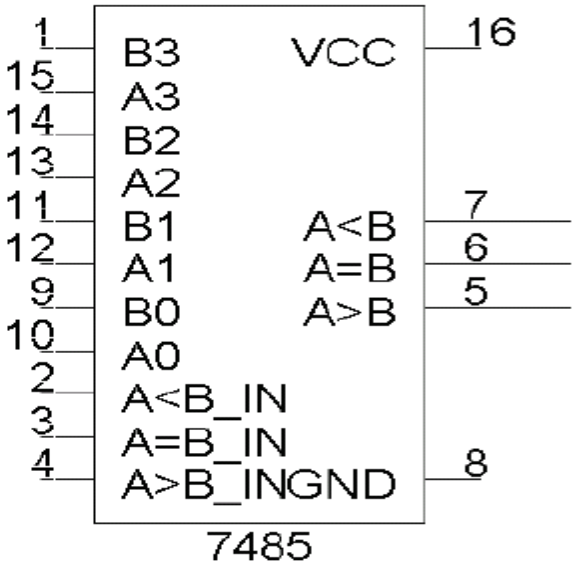
Circuit diagram& truth tables

One Bit Comparator: -



A	B	Y1 (A>B)	Y2 (A = B)	Y3 (A < B)
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

4-bit Comparator



Tabular column :-

A_3 B_3	A_2 B_2	A_1 B_1	A_0 B_0	A>B	A=B	A<B	A>B	A=B	A<B
$A_3>B_3$	X	X	X	X	X	X			
$A_3<B_3$	X	X	X	X	X	X			
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X			
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X			
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X			
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X			
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X			
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X			

Procedure:

1. Interface the Analog Discovery Kit.

2. Complete the connections as per the terminals mentioned in Analog Discovery Kit with IC.
3. Connect the inputs of each logic gate with Analog Discovery Kit and obtain the Timing diagrams.
4. Apply various input combinations, observe and record the output for each pattern/combination and complete the Truth Table.

Result:

Comparator Circuits implemented and truth tables are verified.

11. Flip Flops

Aim:

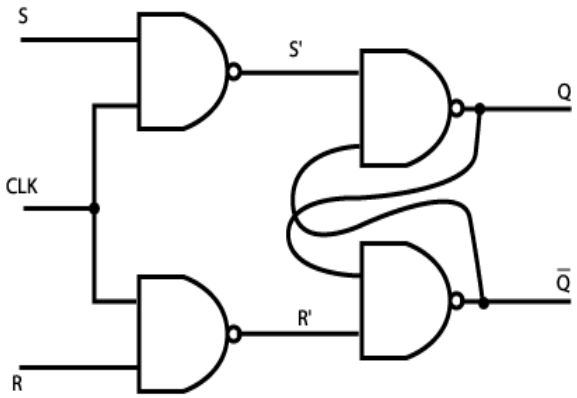
To implement and verify truth table for S-R, J-K, D and T flip-flops.

Apparatus:

Analog Discovery Kit
Bread board
Logic gates / IC's (No. specified or its equivalent GATES):
IC 7400, IC 7404
Connecting Wires

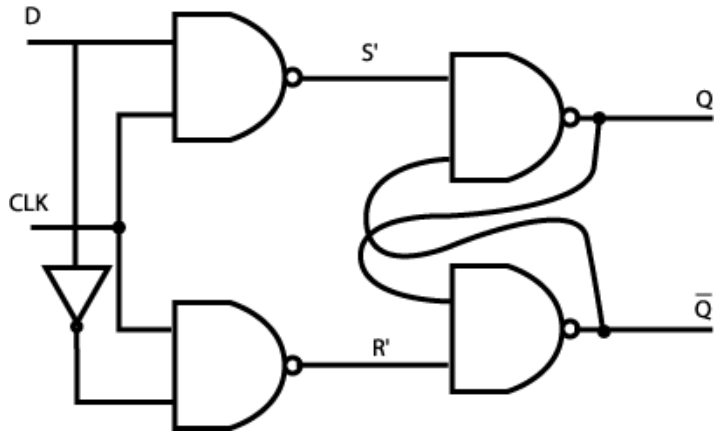
Circuit Diagrams & Truth tables:

i) SR Flip-Flop



SR Flip Flop Truth Table			
R	S	Q	Q'
0	0	Q	Q
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	Invalid	Invalid

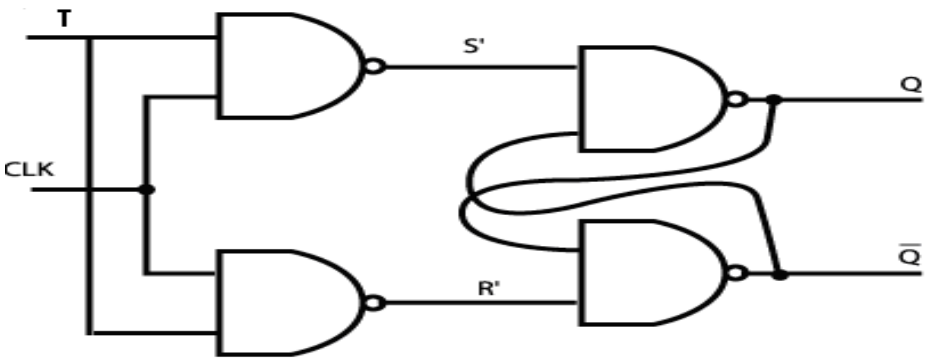
ii) D Flip-Flop



D Flip-Flop:-

Preset	Clear	D	Clock	Qn+1	$\overline{Qn+1}$
1	1	0	⎍	0	1
1	1	1	⎍	1	0

iii) T Flip-flop

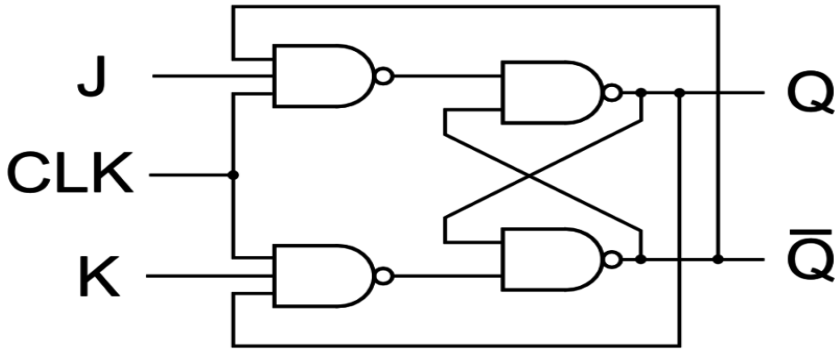


T Flip-Flop:-

Preset	Clear	T	Clock	Qn+1	$\overline{Qn+1}$
1	1	0	⎍	Qn	$\overline{Qn}$
1	1	1	⎍	$\overline{Qn}$	Qn

.

iv) JK Flip-flop



Inputs			Output Q_{n+1}	Operation
CLK	J	K		
0	X	X	Q_n	No change
↓	0	0	Q_n	No change
↓	0	1	0	Reset
↓	1	0	1	Set
↓	1	1	$Q_{n,,}$	Toggles

Procedure:

1. Interface the Analog Discovery Kit.
2. Complete the connections as per the terminals mentioned in Analog Discovery Kit with IC.
3. Connect the inputs of each logic gate with Analog Discovery Kit and obtain the Timing diagrams.
4. Apply various input combinations, observe and record the output for each pattern/combination.
5. Complete the Truth Table for each input/output combination and justify with the operation for each flip flop.

Result:

S-R, J-K, D and T flip-flops are implemented and Truth Tables are verified.

12. JK Flip Flop Master-slave

Aim:

To implement JK Master Slave Flip flop and verify the truth table.

Apparatus:

Analog Discovery Kit
Bread board
Logic gates / IC's (No. specified or its equivalent GATES):
IC 7400, IC 7404
Connecting Wires

Circuit Diagram & Truth table:

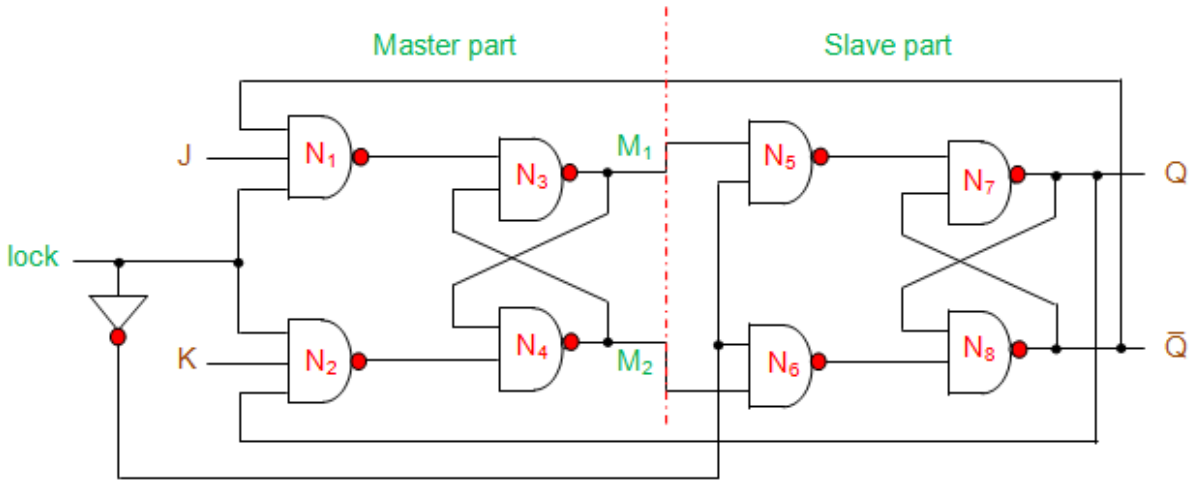


Figure 2 Master-Slave JK flip-flop realized using NAND gates and an inverter

Theory:

The internal structure of a master-slave JK flip-flop interms of NAND gates and an inverter (to complement the clock signal) is shown in Figure 2. Here it is seen that the NAND gate 1 (N_1) has three inputs viz., external clock pulse (Clock), input J and output $\bar{Q}$; while the NAND gate 2 (N_2) has external clock pulse (Clock), input K and output Q as its inputs.

Further the outputs of N_1 and N_2 gates are connected as the inputs for the criss-cross connected gates N_3 and N_4. These four gates together (N_1, N_2, N_3 and N_4) form the master-part of the flip-flop while a similar arrangement of the other four gates N_5, N_6, N_7 and N_8 form the slave-part of it.

From figure it is also evident that the slave is driven by the outputs of the master (M_1 and M_2), which is in accordance with its name **master-slave flip-flop**. Further the master is active during the positive edge of the clock due to which M_1 and M_2 change their states; depending on the values of J and K. However at this instant the outputs of the overall system (master-slave JK flip-flop) remains unchanged as the slave will be inactive due to positive-edge of the clock pulse. Similar to this, the slave decides on its outputs Q and $\bar{Q}$ depending on its inputs M_1 and M_2, during the negative edge of the clock during which the master will be inactive.

The truth table corresponding to the working of the flip-flop shown in Figure 2 is given by Table I. Here it is seen that the outputs at the master-part of the flip-flop (data enclosed in red boxes) appear during the positive-edge of the clock (red arrow). However at this instant the slave-outputs remain latched or unchanged. The same data is transferred to the output pins of the master-slave flip-flop (data enclosed in blue boxes) by the slave during the negative edge of the clock pulse (blue arrow). The same principle is further emphasized in the timing diagram of **master-slave flip-flop** shown by Figure 3. Here the green arrows are used to indicate that the slave-output is nothing but the master-output delayed by half-a-clock cycle.

Truth Table

Trigger	Inputs		Output						Inference
			Present State		Intermediate		Next State		
CLK	J	K	Q	$\bar{Q}$	M_1	M_2	Q	$\bar{Q}$	
↑	0	0	0	1	0	1	Latched		No Change
↓			0	1	Latched		0	1	
↑			1	0	1	0	Latched		
↓			1	0	Latched		1	0	
↑	0	1	0	1	0	1	Latched		Reset
↓			0	1	Latched		0	1	
↑			1	0	0	1	Latched		
↓			1	0	Latched		0	1	
↑	1	0	0	1	1	0	Latched		Set
↓			0	1	Latched		1	0	
↑			1	0	1	0	Latched		
↓			1	0	Latched		1	0	
↑	1	1	0	1	1	0	Latched		Toggles
↓			0	1	Latched		1	0	
↑			1	0	0	1	Latched		
↓			1	0	Latched		0	1	

Table I Truth table for master-slave JK flip-flop

Procedure:

1. Interface the Analog Discovery Kit.
2. Complete the connections as per the terminals mentioned in Analog Discovery Kit with IC.
3. Connect the inputs of each logic gate with Analog Discovery Kit and obtain the Timing diagrams.
4. Apply various input combinations, observe and record the output for each pattern/combination.
5. Complete the Truth Table for each input/output combination and justify with the operation for each flip flop.

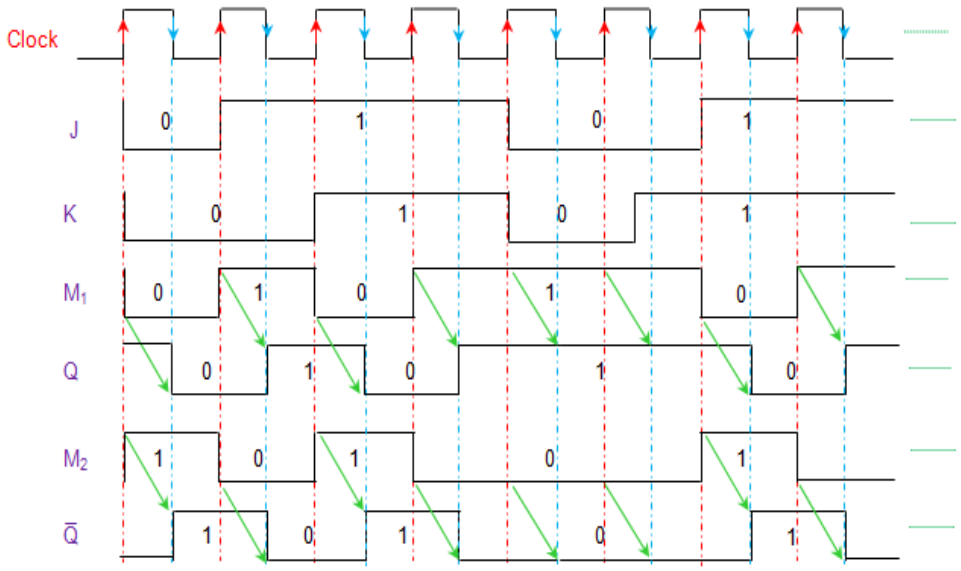


Figure 3 Timing diagram for master-slave JK flip-flop

Result:

Implementation and verification of truth table for J-K flip-flop, Master-slave completed.